MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 3, 2022/23

ECE4116 DIGITAL COMPUTER DESIGN

(All Section / Groups)

06 OCTOBER 2023
9:00 a.m. – 11:00 a.m.
(2 hours)

INSTRUCTIONS TO STUDENT

1. This Question paper consists of 4 pages, including the cover page and with 4 Questions only.

2. Attempt **ALL** questions. All questions carry equal marks, and the distribution of the marks for each question is given.

3. Please print all your answers in the Answer Booklet provided.

Question 1

(a) The Boolean function of a logic circuit is given as:

$F(w, x, y, z) = \sum m(3, 5, 6, 7, 8, 12, 13, 14)$

(i) Construct the truth table for this logic circuit. [4 marks]

(ii) Build the logic circuit by connecting the required logic gates to a 4-to-1 line multiplexer. Connect the multiplexer's selection line to the w and x inputs..

[6 marks]

(b) Write a VHDL behavioral architecture code for a positive-edge triggered D-type flip flop with active high reset input.

[3 marks]

(c) The following input equation represents a sequential circuit consisting of two D flip-flops, A and B, with inputs Y and output Z.

$$D_A = BY + \bar{A}Y, D_B = \bar{Y}, Z = \bar{A}\bar{B}$$

(i) Draw this sequential circuit. [4 marks]

(ii) Construct its state table. [4 marks]

(iii) Draw its state diagram. [4 marks]

Question 2

(a) Make TWO (2) control-function-using register transfer statements represent the following conditional control statement:

If (X=1) then ($R1 \leftarrow R2$) else if (Y=1) then ($R1 \leftarrow R3$) [3 marks]

(b) Implement the following operation using two 4-bit registers, R1 and R2, and the correct logic gates, in a single bit slice of the logic diagram.

C_0: $R2 \leftarrow R1$ Transfer $R1$ to $R2$

C_1: $R2 \leftarrow \overline{R2}$ Complement $R2$

C_2: $R2 \leftarrow 0$ Clear $R2$

One of the control variables can be set to 1 at any one time while the other two are always set to 0. [9 marks]

(c) List THREE (3) basic arithmetic microoperations and provide an example using register transfer statement for each of them. [3 marks]

(d) Multiple 256K × 8 RAM chips are used to construct a 4Mbytes RAM.

(i) Determine the number of 256K × 8 RAM chips that are needed. [2 marks]

(ii) Compute the number of address lines needed for each 256K × 8 RAM chip. [2 marks]

(iii) Compute the number of address lines required to access the 4MBytes RAM. [2 marks]

(iv) Determine the number of address lines that must be decoded to produce the chip select input and specify the size of the decoder. [4 marks]

Continued...

Question 3

(a) Figure Q3 (a) depicts a functional table for an arithmetic circuit. 16-bit data streams (A and B) and control signals (S0 and S1) make up the inputs. F, a 16-bit value, is shown as the result.

$S1$	$S0$	Function
0	0	$F = A$ (transfer)
0	1	$F = A + B$ (addition)
1	0	$F = A + \bar{B} + 1$ (subtraction)
1	1	$F = A + 1$ (increment)

Figure Q3(a)

Two data inputs (X and Y), an output (S), a carry-in (Cin) and a carry-out (Cout) make up the arithmetic circuit's parallel adder. X input is for data A, and Y input is for data B. Additional logic is needed to implement the functions shown in Figure Q3a when the Y input is included..

(i) Write the truth table for *X*, *Y*, and *Cin* input values in terms of *A*, *B*, *S0*, and *S1*.

[4 marks]

(ii) Based on the truth table in (i), write the Boolean expressions for *X*, *Y* and *Cin* inputs.

[3 marks]

(iii) *Y* input logic is implemented using a 4-to-1 multiplexer. Draw the complete circuit block diagram for the arithmetic circuit.

[6 marks]

(b) An instruction is stored at location 550 with its address field at location 551. The address field has the value 2410, as sown in Figure Q3(b). A processor register *R1* contains the value 2310. All values are shown in **decimal**. Evaluate the effective address for each of the following addressing modes:

(i) Direct. [2 marks]

(ii) Immediate. [2 marks]

(iii) Relative. [2 marks]

(iv) Indexed (using register *R1* as the index register). [2 marks]

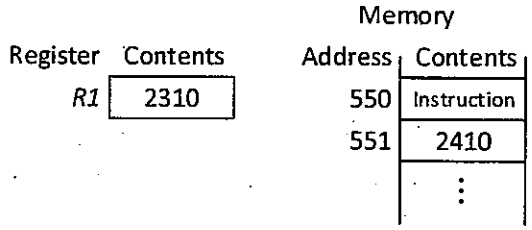

Figure Q3(b)

Continued...

(c) A computer has a 32-bit word length; all instructions are one word in length with no mode field. The register file of the computer has 64 registers.

(i) For instruction with three register addresses and an 8-bit constant field, determine the maximum number of possible opcodes. [2 marks]

(ii) For an instruction format with two register addresses, one constant field and a maximum of 64 opcodes, what is the number of bits available for the constant field? [2 marks]

Question 4

(a) For the barrel shifter shown in Figure Q4(a), if A is given as $13579ABC_{16}$, list the hexadecimal values on the 47 lines, 35 lines, and 32 lines out of the three levels of the shifter for the following shift:

Right, $SH = 0F_{16}$ [8 marks]

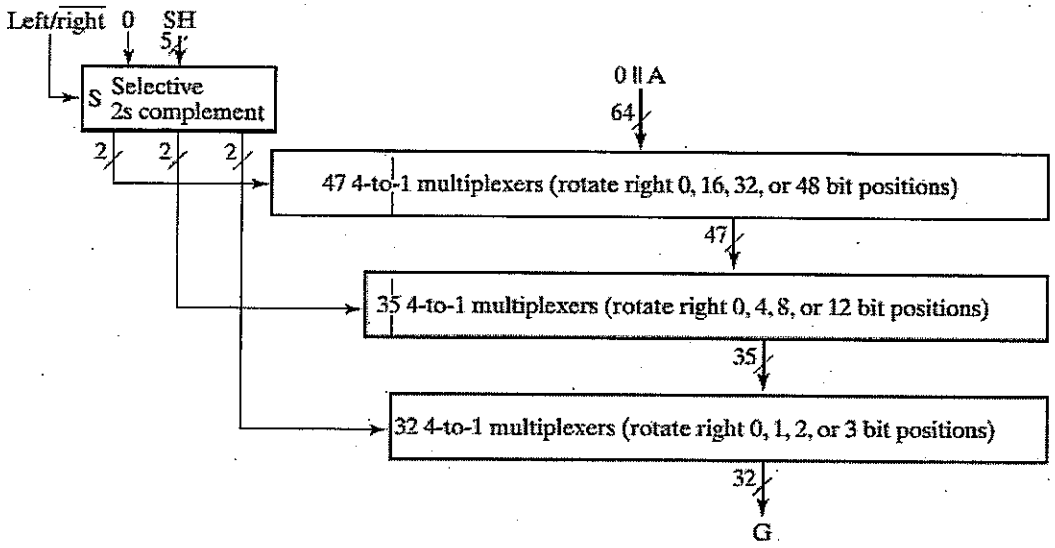

Figure Q4(a)

(b) A hypothetical RISC machine employs a typical 4-stage pipeline. The following sequence of instructions is executed.

```
MOVA    R1, R5
SLT     R2, R4, R1
BNZ     R2, 25
MOVA    R5, R8
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Continued...

(i) Draw the pipeline execution diagram to show the execution of the instructions. Subsequently, identify all hazards and specify what type they are?

[8 marks]

(ii) Describe the methods to resolve the hazards identified in part (i).

[6 marks]

(c) CISC machines have complex instructions, some of which require more than one execution cycle to complete. This characteristic makes it unsuitable for standard pipelining. Describe the modification that allows the implementation of a 4-stage pipeline for a CISC machine.

[3 marks]

End of Paper